Credo Announces 3.2Tbps XSR-Enabled High-Speed Connectivity Chiplet with 112Gbps Lane Rates

May 19, 2021

Advanced Low Power Mixed-Signal DSP Technology Enables 32x112G Full-Duplex Chiplet for High Performance, Low Power MCM ASIC Solutions for Advanced Switching, Compute, Artificial Intelligence, Machine Learning, and next-generation Co-Packaged Optics solutions (CPO)

San Jose, Calif., May 18, 2021 – **Credo**, a global innovation leader in advanced connectivity solutions delivering high performance, low power connectivity solutions for 100G, 400G, and 800G port-enabled networks, today announced the production availability of Nutcracker, the industry's first low-power 3.2Tbps retimer XSR-enabled high-speed connectivity chiplet with 112Gbps lane rates. The new device is optimized for low power and system reach performance in next-generation multi-chip-modules (MCM) ASICs for advanced switching, compute, artificial intelligence, machine learning, and CPO applications.

Nutcracker has 32 low-power lanes of 112G XSR SerDes on the host side, which communicate with the in-module system-on-chip (SOC) core ASIC. The chiplet has 32 lanes of low-power 112G MR+ reach-optimized DSP to provide the off-module interface on the line side.

Credo's unique DSP technology allowed the development of the low-power 32x112Gbps XSR to 32x112Gbps MR+ retimer die in TSMC's 12nm process. In contrast, alternative solutions will require the usage of more costly 7nm or 5nm nodes.

Credo optimized the architecture to enable SOC ASIC providers to maximize their core processing functionality through the area- and power-efficient XSR interfaces. Nutcracker delivers a robust, off-package interface for the MCMs, which allows for easy integration in various system-level configurations.

Integrating chiplets into MCM designs accelerates ASIC innovation required to meet the increasing performance demands of switching, storage, service providers, high-performance computing, artificial intelligence, and machine learning devices.

"We developed and commercialized Nutcracker in a strategic collaboration with a large, Fortune 200 customer," said Jeff Twombly, Vice President of Business Development at Credo. "Nutcracker is now the leading solution for next-generation ASIC deployments requiring heterogeneous MCM approaches to achieve the performance scale demanded across all technology industries, including emerging co-packaged optics in the data center," Twombly continued.

"Credo's Nutcracker XSR chiplet is an important building block to next-generation ASIC designs. As the data center market moves toward higher speed 400G, 800G and beyond ASICs, the market will transition away from monolithic ASICs to MCM solutions," said Alan Weckel, Founder and Technology Analyst at 650 Group. "As the market moves towards 25.6Tbps and 51.2Tbps, we expect many ASICs to make the transition towards multi-chip-modules," Weckel concluded.

Nutcracker will be demonstrated at the 2021 TSMC Online Innovation Zone. Videos of the demonstration will be on Credo's website following the event. The Nutcracker device is in production.

For more information about Nutcracker and other industry-leading Credo connectivity solutions, visit **https://www.credosemi.com/serdes-ip-and-chiplets**.

About Credo

Credo is a leading provider of high-performance serial connectivity solutions for the hyperscale datacenter, 5G carrier, enterprise networking, artificial intelligence, and high-performance computing markets. Credo's solutions deliver the bandwidth, scalability, and end-to-end signal integrity for next-generation platforms requiring 25G, 50G, and 100G signal lane-rate connectivity for 100G, 200G, 400G, and 800G port enabled networks.

For more information, please visit **https://www.credosemi.com**. Follow Credo on **LinkedIn** and **Twitter**.