Open-Silicon, Credo and IQ-Analog Showcase Complete End-to-End Networking ASIC Solutions at OFC 2018

March 12, 2018

San Diego, CA, March 12, 2018 | Open-Silicon, Credo and IQ-Analog will participate in joint demonstrations at the Optical Fiber Communications Conference (OFC) 2018 in San Diego, CA on March 13-15. The companies will showcase their complete end-to-end ASIC solutions for leading-edge networking applications, such as long-haul, metro and core, broadband access, optical, carrier IP and data center interconnect. Open-Silicon will present its ASIC offerings as well as its comprehensive Networking IP Subsystem Solution, which includes high-speed chip-to-chip interface Interlaken IP, Ethernet Physical Coding Sublayer (PCS) IP, FlexE IP compliant to OIF Flex Ethernet standard v1.0 and v2.0, and Multi-Channel Multi-Rate Forward Error Correction (MCMR FEC) IP. Open-Silicon will also demonstrate its High Bandwidth Memory (HBM2) IP Subsystem Solution. Credo will demonstrate its high-speed 56Gbps PAM4 LR Multi-Rate SerDes solution and 112Gbps PAM4 SR/LR SerDes targeted for next generation networking ASICs. IQ-Analog will showcase its high-performance analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

“This collaborative demonstration with our partner companies is an excellent opportunity to unveil the power of a complete end-to-end solution for the next generation of high performance networking applications,” said Taher Madraswala, President and CEO of Open-Silicon. “Having representatives from all three companies in one place also presents a unique opportunity for attendees to discuss their ideas and unique design requirements.”

“Credo's silicon proven 56G/112G SerDes IPs, combined with Open-Silicon's SerDes technology center of excellence, can minimize risk and time-to-market for developing the next generation of networking and data center ASICs,” added Bill Brennan, President and CEO of Credo.

“IQ-Analog’s patented TPWQ hyper-speed 90Gsps ADC/DAC IPs, combined with Open-Silicon’s robust physical design methodology, enables development of the next generation of carrier IP and optical networking ASICs with industry leading power, area and performance,” said Mike Kappes, President and CEO of IQ-Analog.

When: March 13–15, 10 A.M. to 5 P.M.

Where: Exhibit Floor, **Booth # 6307**, San Diego Convention Center, San Diego, CA, USA

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