Credo Unveils Robust Portfolio of 56G and 112G PAM-4 PHY Connectivity Solutions

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High-Performance, Low-Power Devices Enable Data Center Scalability to 50G, 100G, 200G, 400G and Beyond

Milpitas, Calif., May 8, 2017 – Credo Semiconductor, a global innovation leader in Serializer-Deserializer (SerDes) technology, today announced a comprehensive portfolio of 56G and 112G PAM-4 PHY devices, enabling connectivity for enterprise, hyperscale datacenter, and service provider networks. Leveraging Credo's unique, patented mixed signal processing technology, the new PHY devices deliver industry-leading performance and low power. This unique approach avoids the need for power-hungry DSP SerDes architectures and the requirement to be on the most advanced processing nodes. Credo has also leveraged its low latency, low power forward error correction (FEC) technology to guarantee end-to-end, error-free performance as networks transition from 25G to 50G and 100G single-lane rates.

"Our new portfolio has been developed to meet the bandwidth requirements of the next generation of hyperscale datacenter buildouts," said Jeff Twombly, vice president of business development for Credo. "With a unique architecture that delivers the best of both analog and digital approaches, these new 56G and 112G PHY devices achieve power and performance targets in 28nm that have not been possible with competitive approaches. This means that we are able to meet stringent customer requirements while leveraging more cost-effective process nodes."

"As manufacturers begin to develop equipment for emerging hyperscale data centers, they not only need guarantees of error-free transmission from their PHYs, but also want to build their systems and networks as efficiently as possible," said Simon Stanley, principal consultant at Earlswood Marketing. "Architectures that can meet the power and performance requirements of next-generation networking equipment without having to move to smaller geometries have the potential to reduce time, cost and risk for these manufacturers."

The Credo connectivity solutions are optimized for a range of applications. The optical family is focused on QSFP28, QSFP56, QSFP-DD, and OSFP pluggable modules supporting standards such as DR1, 2xDR1, DR4, FR4, FR8, and CWDM8. The copper family provides designers with a range of solutions to deliver robust signal integrity connections for backplane, front-panel and ACC.

Credo Optical Connectivity:

- CMX125100P - 100G (4x28G NRZ to 1x112G PAM-4 PHY) for QSFP28 (i.e., DR1)
- CMX225100P - 200G (8x28G NRZ to 2x112G PAM-4 PHY) for QSFP-DD, OSFP (i.e., 2xDR1)
- CMX450100P - 400G (8x56GG PAM-4 to 4x112G PAM-4 PHY) for QSFP-DD, OSFP (i.e., DR4, FR4)
- CRT5014P - 400G (4x56G PAM-4 to 4x56GG PAM-4) for QSFP56 (i.e., CWDM4)
- CRT5018P - 400G (8x56G PAM-4 to 8x56GG PAM-4) for QSFP-DD, OSFP (i.e., FR8, CWDM8)

Credo Copper Connectivity:

- CMX22550P - 200G (4x56G PAM4 to 8x28G NRZ PHY) for backplanes and line cards
- CMX42550P - 400G (8x56G PAM4 to 16x28G NRZ PHY) for backplanes and line cards
- CRT5024P - 200G (4x56G PAM4 PHY to 4x56G PAM4 PHY) for servers, NIC, and line cards
- CRT5028P - 400G (8x56G PAM4 PHY to 8x56G PAM4 PHY) for backplanes and line cards
- CRT50216P - 800G (16x56G PAM4 PHY to 16x56G PAM4 PHY) for backplanes and line cards

Several members of the Credo connectivity family are sampling and Credo has evaluation platforms to validate in-system performance. Please contact sales@credosemi.com for more information.

About Credo Semiconductor

Credo is a leading provider of high performance, mixed-signal semiconductor solutions for the data center, enterprise networking and high performance computing markets. Credo's advanced Serializer-Deserializer (SerDes) technology delivers the bandwidth scalability and end-to-end signal integrity for next generation platforms requiring single-lane 25G, 50G, and 100G connectivity. Credo has offices in Milpitas, California, Shanghai, and Hong Kong. For more information: www.credosemi.com