Credo 16-nm 56G PAM-4 SerDes IP Now Available

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Delivers Advanced IP on the TSMC 16-nm FinFET+ Process

Milpitas, Calif., March 14, 2016 – Credo Semiconductor, a global innovation leader in Serializer-Deserializer (SerDes) technology, today announced that its 56Gbps PAM-4 SerDes IP is available for the TSMC 16-nm FinFET+process. Based on Credo's unique analog architecture that delivers low power and high performance, the new SerDes IP can be leveraged by ASIC, SoC and systems designers to dramatically increase bandwidth in data centers, enterprise networks, and high-performance computing applications.

"We continue to provide our high-profile semiconductor and networking customers a migration path to the industry's fastest data rates with cutting-edge performance and extremely low power,"said Jeff Twombly, vice president of business developmentat Credo. "Credo's unique analog architecture delivers a compelling solution for optimizing power and performance as our customers move from single-lane 28G connections to single-lane 56G connections. As important, our solutions enable innovations at the sytem level that meet the accelerating demand for higher bandwidth in data centers."

Credo has demonstrated its solution by driving a 56G PAM-4 signal, error free,across a variety of copper cable lengths. Credo also has a wide range of previously announced 28G and 56G SerDes IP available.

Supporting the speed and modulation schemes in definition by emerging IEEE and OIF CEI standards, the new Credo 56G PAM-4 SerDes IP is ideal for use in next-generation chip-to-chip, chip-to-module, chip-to-backplane and cable solutions targeting 100G and 400G networks. It can also be used in existing networks to provide 10G, 25G, 40G and 50G connectivity with extended reach.

AVAILABILITY AND DELIVERABLES

The Credo 56G PAM-4 SerDes IP is available now on the TSMC 16-nm FinFET+ process and is expected to be available Q2 2016 on the TSMC FinFET Compact (FFC) process. Deliverables include user and SoC integration guides; netlist; timing library; register map; Verilog, ATPG, and IBIS-AMI models; LEF views; Layout Versus Schematic (LVS) and Design Rule Check (DRC) reports.

Companies interested in learning more about the company's current silicon and intellectual property engagement options, as well as future developments, should contact sales@credosemi.com.

ABOUT CREDO SEMICONDUCTOR

Credo is a leading provider of high performance, mixed-signal semiconductor solutions for the data center, enterprise networking and high performance computing markets. Credo's advanced Serializer-Deserializer (SerDes) technology delivers the bandwidth scalability and end-to-end signal integrity for next generation platforms requiring single-lane 25G, 50G, and 100G connectivity. The company makes its SerDes available in the form of Intellectual Property (IP) licensing on the most advanced processing nodes and with complementary product families focused on extending reach and multiplexing to higher data rates. Credo is headquartered in Milpitas, California and has offices in Shanghai and Hong Kong. For more information: www.credosemi.com.